XA-9629
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Yutaka SHIMADA et al.

Appln. No.:

Filed: HEREWITH

For: MANUFACTURING METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

* * *

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to 37 C.F.R. § 1.56, and without any assertion as to materiality or prior art effect, the documents listed on the attached Form PTO-1449 are hereby cited.

The documents on the attached List are cited in the specification, on pages 2-4, and their relevance is indicated therein.

Respectfully submitted,

MWS:sjk

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By: _____
Mitchell W. Shapiro
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February 27, 2002